

USPTO
00/62/00

10-2-00

A

PATENT APPLICATION TRANSMITTAL LETTER
(Large Entity)

Docket No.
INTL-0444-US (P9444)

TO THE ASSISTANT COMMISSIONER FOR PATENTS

Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

MINDA ZHANG and PRANAV H. MEHTA

For: **ENABLING SECURE COMMUNICATIONS WITH A CLIENT**

Enclosed are:

- Certificate of Mailing with Express Mail Mailing Label No. **EL661130439US**
- Five (5) sheets of drawings.
- A certified copy of a application.
- Declaration Signed. Unsigned.
- Power of Attorney
- Information Disclosure Statement
- Preliminary Amendment
- Other: Recordation Form Cover Sheet; Assignment and check for \$40.

jc564 U.S. PTO
09/676068
09/29/00

CLAIMS AS FILED

For	#Filed	#Allowed	#Extra	Rate	Fee
Total Claims	30	- 20 =	10	x \$18.00	\$180.00
Indep. Claims	4	- 3 =	1	x \$78.00	\$78.00
Multiple Dependent Claims (check if applicable)					\$0.00
				BASIC FEE	\$690.00
				TOTAL FILING FEE	\$948.00

- A check in the amount of **\$948.00** to cover the filing fee is enclosed.
- The Commissioner is hereby authorized to charge and credit Deposit Account No. **20-1504** as described below. A duplicate copy of this sheet is enclosed.
 - Charge the amount of as filing fee.
 - Credit any overpayment.
 - Charge any additional filing fees required under 37 C.F.R. 1.16 and 1.17.
 - Charge the issue fee set in 37 C.F.R. 1.18 at the mailing of the Notice of Allowance, pursuant to 37 C.F.R. 1.311(b).

Dated: **September 29, 2000**



Signature
Timothy N. Trop, Reg. No. 28,994

TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
Phone: (713) 468-8880
Fax: (713) 468-8883


021906

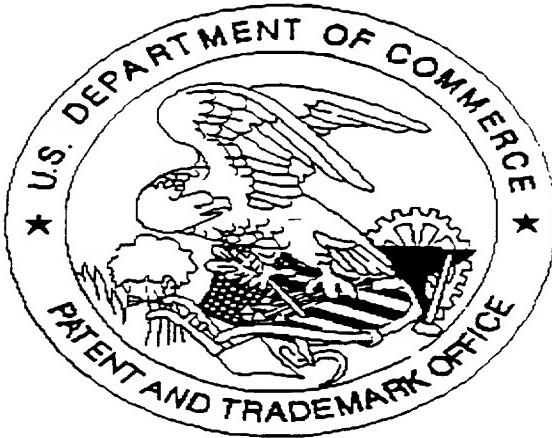
cc:

Customer No. 21906

PATENT AND TRADEMARK OFFICE

P01LARGE/REV07

United States Patent & Trademark Office
Office of Initial Patent Examination -- Scanning Division



Application deficiencies were found during scanning:

Page(s) _____ of Express Mailing _____ were not present
for scanning. (Document title)

Page(s) _____ of _____ were not present
for scanning. (Document title)

Scanned copy is best available.

INTL-0444-US
(P9444)

APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: ENABLING SECURE COMMUNICATIONS WITH A
CLIENT

INVENTORS: MINDA ZHANG and PRANAV H. MEHTA

Express Mail No.: EL661130439US

Date: September 29, 2000

ENABLING SECURE COMMUNICATIONS WITH A CLIENT

Background

This invention relates generally to enabling secure communications between an head end or server and a receiving client, for example in systems that distribute television content, software or other content electronically.

In a digital broadcast system, digital content may be transmitted from a head end or server to a plurality of receivers or clients. Ideally, the system is secure enough to prevent hackers from intercepting the content and viewing it without paying for the content. Similarly, other electronic communications may be sent in the same fashion including application programs as another example.

In each case, conditional access services may be provided using a device key to enable secure communications between the head end and the client. One approach to providing such a system is to use a smart card reader at the client. However, the smart card system can be hacked since it is possible to obtain the information from the smart card and then to use it to receive the services for free. The hacker merely monitors the smart card interface. The hacker may thereafter use computing resources to decipher the data using a distributed attacking scheme and

distribute a control word such as a session key in real time over the Internet.

Similar approaches involve installing a unique device key into a flash memory or an electrically erasable programmable read only memory (EEPROM) as an alternative to a smart card. An encryption scheme may be used to pass the device key into a transport demultiplexer or other conditional access service receiver before receiving conditional access services. However, the standalone, non-volatile memory device may easily be removed and replaced by a hacker.

As another approach, a unique device key may be integrated into a non-volatile memory device that is part of the transport demultiplexer module. However, the drawback of such an approach is a lack of renewability of the device key and the relatively higher manufacturing cost.

Still another approach is to have a manufacturer key burned into the transport demultiplexer at the client. The head end then generates and sends the device key covered by the manufacturing key to each client. Although this approach provides an effective way to renew the device key, it enables those clients with the same manufacturer key to steal the device key when the head end sends the key down to the client who subscribes to the broadcasting service.

Thus, there is a need for better ways to secure transmissions between a head end and a client that enables the device key to be renewed while reducing the likelihood of a device key being intercepted.

5

Brief Description of the Drawings

Figure 1 is a block diagram of hardware in accordance with one embodiment of the present invention;

10 Figure 2 is a chart that shows the flow for developing the device key and providing it to a head end in accordance with one embodiment of the present invention;

Figure 3 is a flow chart for generating a digital certificate in accordance with one embodiment of the present invention;

15 Figure 4 is a flow chart for developing a device key in accordance with one embodiment of the present invention; and

Figure 5 is a flow chart for software for renewing a device key in accordance with one embodiment of the present invention.

20

Detailed Description

A receiver or client 10, shown in Figure 1, may receive conditional access services via an input device 46 such as an antenna, a cable connection, a satellite receiver or an Internet connection, as examples. The 25 services may be digital broadcast services, application

program services or other electronic data or content. The client 10 may include a processor 12. Advantageously, the processor 12 has a unique processor identifier or serial number called a CPUID and implements instructions to

5 provide the CPUID at the operating system kernel level upon request. One such processor is the Pentium® III processor available from Intel Corporation, Santa Clara, California.

The processor 12 couples to a north bridge 14 that in turn is coupled to a graphics chip 16 and a host memory 18.

10 The graphics chip 16, in one embodiment of the present invention, may be coupled to a television or other audio/video output device.

The north bridge 14 is coupled to a bus 20 that couples to a south bridge 22. The south bridge 22 may be

15 coupled to a non-volatile memory 24 such as a flash memory. In one embodiment of the present invention, the memory 24 may store a basic input/output system (BIOS). The memory 24 may also store a device key that is used to convert

20 between plain text and cipher text in accordance with one embodiment of the present invention. A hard disk drive 26 may also be coupled to the south bridge 22. The hard disk

drive 26 may store software 50 and 80 for implementing conditional access services in accordance with one embodiment of the present invention.

25 The bus 20 is also coupled to a chip or integrated circuit 28. In one embodiment, the integrated circuit 28

may include a transport demultiplexer 34 and a key logic 36 integrated into the same semiconductor die. Thus, one can not readily intercept communications between the key logic 36 and the transport demultiplexer 34. In one embodiment 5 of the present invention, the device key may be stored in a memory 35 in the transport demultiplexer 34. The integrated circuit 28 also includes a bridge 30 that couples the circuit 28 to the bus 20. In some embodiments, the circuit 28 may include its own bus 32 that couples the key logic 36 10 and the transport demultiplexer 34. A smart card interface 38 and smart card 40 may also be provided in some embodiments.

The integrated circuit 28 may be coupled to a demodulator 42 and a tuner 44 that receive input signals 15 from the head end or server via the input device 26. Thus, in a digital broadcasting embodiment the transport demultiplexer 34 demultiplexes the digital broadcast information received from the head end. The client 10 may only demultiplex the information if the client 10 is 20 authorized to receive such broadcasts as determined by the cooperation of the processor 12, the key logic 36 and the memory 24 in a fashion described in more detail hereinafter.

Referring to Figure 2, the processor 12 initiates the 25 procedure of developing the device key for transmission to the head end so that the head end can provide conditional

access services to the client 10. The processor 12 requests a random challenge or random number. In one embodiment of the present invention, the random number is generated by the key logic 36. The random number or random challenge is then transmitted back to the processor 12. At the same time, the processor 12 generates a device key seed or starting value that may be a 64-bit value in one embodiment. The device key seed may then be sent by the processor 12 to the memory 24. The device key seed, originally stored in the memory 24, may be replaced with the device key seed generated by the processor 12.

The device key seed received from the memory 24 is then sent back to the processor 12. At the operating system kernel level, the processor 12 executes the CPUID instruction, reads the device key seed from the memory 24 and generates a certificate. Thus, at the operating system kernel level (which is generally inaccessible to application programs), the processor 12 uses its own CPUID instructions to obtain its own unique serial number, obtains the device key seed from the memory 24 and hashes all this information to generate a secure certificate. Public key or symmetric key based cipher systems may be used to generate the secure certificate. However, the underlying signing key may be based on the unique CPUID. The routine for generating the secure certificate may be protected using tamper resistant software (TRS) agents.

The certificate is then sent by the processor 12 to the key logic 36. The certificate ensures secure communications between the processor 12 and key logic 36. The key logic 36 validates the certificate and processes 5 the certificate to generate a new device key. Moreover, the key logic 36 encrypts the new device key using the current device key and then writes the cipher text back to the host processor 12. In addition, the cipher text of the new device key may be written to the head end by the 10 processor 12 in order for the head end to update its database of device keys for various clients 10.

The software 50, shown in Figure 3, for generating the certificate, in one embodiment, may begin by requesting a random challenge from the key logic 36, as indicated in 15 block 52. The processor 12 then receives the random challenge from the key logic 36, as indicated in block 54. The processor 12 also executes its CPUID instructions as indicated in block 56 in order to obtain its own unique serial number.

20 Thereafter, the processor 12 reads the device key seed from the memory 24 as indicated in block 58. Using the device key seed, the CPUID, and the random number challenge, the processor 12 generates a digital signature as indicated in block 60. The digital signature or 25 certificate is then written into the integrated circuit 28 at the application level as indicated in block 62. In this

way, the integrated circuit 28 can be sure that the communications it is receiving are authentic and that a hacker is not attempting to substitute a new device key for the actual device key.

5 Referring next to Figure 4, the software 64, in one embodiment, for generating a device key in the key logic 36 initially verifies the digital signature received from the processor 12 as indicated in block 66. The CPUID received and the device key seed received in the digital signature
10 are processed to generate a pseudorandom bit stream (block 68). The new device key is then stored in the memory 35 in the transport demultiplexer 34 as indicated in block 70. Since the key logic 36 and transport demultiplexer 34 are formed in the same integrated circuit 28, it is virtually
15 impossible for a hacker to intercept the communications between the key logic 36 and the transport demultiplexer 34. Alternatively, such communication may also be encrypted.

Turning finally to Figure 5, a new device key may be periodically provided at the request of the head end as
20 indicated in diamond 82. When the processor 12 receives a head end request for a new device key, the processor generates a pseudorandom n-bit value as indicated in block 84. It also requests a new challenge from the key logic 36 as indicated in block 86. When the processor 12 receives
25 the new challenge as indicated in block 88, it generates a certificate as indicated in block 90. The certificate is

written to the key logic 36 as indicated in block 92. The device key is received by the host processor from the key logic 36 as indicated in block 94. The processor 12 sends the cipher text of the device key to the head end as indicated in block 96.

Thus, embodiments of the present invention provide secure communication at reasonable cost. The processor 12 is the core of the platform and its unique serial number is not alterable. Thus, in some embodiments the client 10 may avoid making a copy of the device key anywhere in any non-volatile memory. This significantly reduces the cost of protecting the device key. Also, by executing the CPUID instruction at the operating system kernel level, the client 10 effectively prevents hackers from producing a valid certificate for a known processor serial number. Thus, it is extremely difficult to fool the key logic 36 to produce a valid device key without both the serial number and the device key seed.

While the present invention has been described with respect to a limited number of embodiments, those skilled in the art will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of this present invention.

What is claimed is:

1 1. A method comprising:
2 receiving a processor identifier;
3 receiving a seed stored in a non-volatile memory;
4 and
5 hashing said identifier and said seed to develop
6 a device key.

1 2. The method of claim 1 further including
2 requesting a random number and hashing said identifier and
3 said seed with said random number.

1 3. The method of claim 2 including causing a
2 processor to execute instructions to obtain a processor
3 serial number.

1 4. The method of claim 1 including obtaining said
2 processor identifier by executing instructions at the
3 operating system kernel level.

1 5. The method of claim 2 including causing a
2 processor to obtain a random number from an integrated
3 circuit and generating a certificate.

1 6. The method of claim 5 including causing the
2 processor to send said certificate to said integrated
3 circuit.

1 7. The method of claim including causing said
2 integrated circuit to validate said certificate and process
3 said certificate to generate a device key.

1 8. The method of claim 7 including encrypting a new
2 device key using a current device key and writing the
3 encrypted new device key back to the processor.

1 9. The method of claim 7 including writing said
2 device key into a memory in said integrated circuit.

1 10. The method of claim 1 including receiving a
2 digital television broadcast from a head end and sending
3 said device key to said head end.

1 11. An article comprising a medium storing
2 instructions that enable a processor-based system to:
3 receive a processor identifier;
4 receive a seed stored in a non-volatile memory;
5 and

6 hash said identifier and said seed to develop a
7 device key.

1 12. The article of claim 11 further storing
2 instructions that enable the processor-based system to

3 request a random number and hash said identifier and said
4 seed with said random number.

1 13. The article of claim 12 further storing
2 instructions that enable the processor-based system to
3 execute instructions to obtain a processor serial number.

1 14. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 obtain said processor identifier by executing instructions
4 at ring 0.

1 15. The article of claim 12 further storing
2 instructions that enable the processor to obtain a random
3 number from an integrated circuit and generate a
4 certificate.

1 16. The article of claim 15 further storing
2 instructions that enable the processor-based system to send
3 said certificate to said integrated circuit.

1 17. The article of claim 16 further storing
2 instructions that enable the processor-based system to
3 cause said integrated circuit to validate said certificate
4 and process said certificate to generate a device key.

1 18. The article of claim 17 further storing
2 instructions that enable the processor-based system to
3 encrypt a new device key using a current device key.

1 19. The article of claim 17 further storing
2 instructions that enable the processor-based system to
3 write said device key into a memory in said integrated
4 circuit.

1 20. The article of claim 11 further storing
2 instructions that enable the processor-based system to
3 receive a digital television broadcast from the head end
4 and send said device key to said head end.

1 21. An integrated circuit comprising:
2 an interface to couple said circuit to a
3 processor-based system;
4 a transport demultiplexer coupled to said
5 interface to receive audio/video content information;
6 a key logic circuit to extract a device key from
7 a bit stream including a processor serial number and a
8 device key seed; and
9 a memory to store said device key.

1 22. The circuit of claim 21 wherein said memory is
2 part of said transport demultiplexer.

1 23. The circuit of claim 21 including a bus that
2 couples said interface, said transport demultiplexer and
3 said key logic circuit.

1 24. The circuit of claim 21 wherein said key logic
2 circuit generates a random challenge on request from said
3 processor-based system.

1 25. The circuit of claim 21 wherein said key logic
2 circuit receives a certificate from said processor-based
3 system and processes said certificate to generate a device
4 key.

1 26. The circuit of claim 25 wherein said key logic
2 encrypts a new device key using a current device key.

1 27. A processor-based system comprising:
2 a processor that stores instructions that enable
3 said processor to obtain a processor serial number;
4 a non-volatile memory, coupled to said processor,
5 to store a device key seed;
6 an integrated circuit coupled to said processor,
7 said integrated circuit including a key logic circuit that
8 generates a random challenge upon request from said
9 processor.

1 28. The system of claim 27 wherein said key logic
2 circuit extracts the device key from a bit stream including
3 a processor serial number and a device key seed.

1 29. The system of claim 28 including a memory in said
2 integrated circuit, said key logic circuit enabling said
3 device key to be stored in said memory.

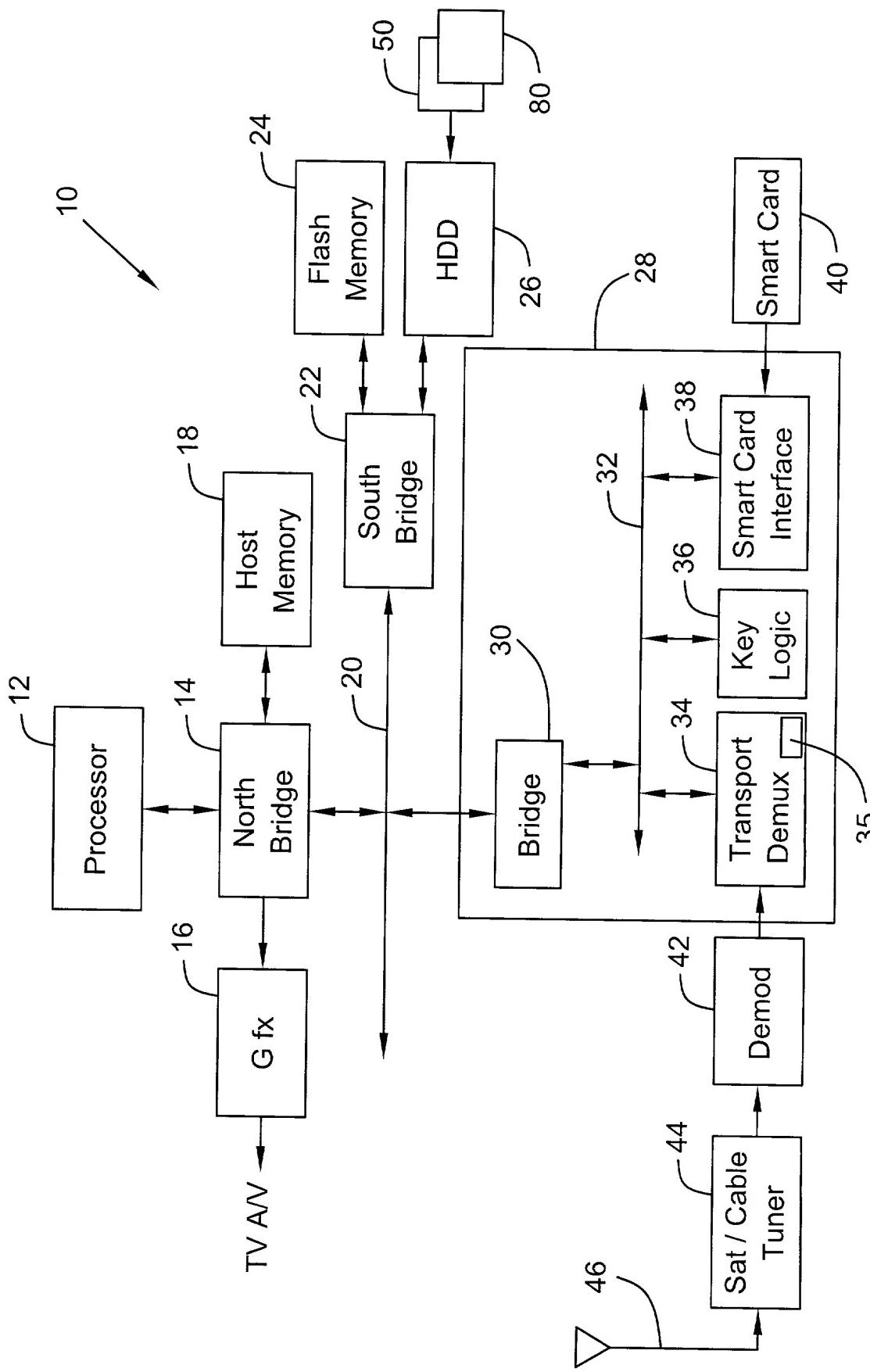
1 30. The system of claim 29 wherein said integrated
2 circuit includes a transport demultiplexer that receives
3 content from an external source, said memory being included
4 as part of said transport demultiplexer.

ENABLING SECURE COMMUNICATIONS WITH A CLIENT

Abstract of the Disclosure

A unique processor serial number may be utilized to augment a device key seed stored in a non-volatile memory. In this way, a relatively secure system may be enabled that 5 facilitates renewing the device key. An integrated circuit may include a transport demultiplexer and key logic. The key logic communicates with the processor using a secure protocol. The key logic can generate random numbers that may be hashed with the processor serial number and the 10 device key seed to generate a device key. The device key may be provided to a head end to facilitate secure communications between the head end and the client.

FIG. 1



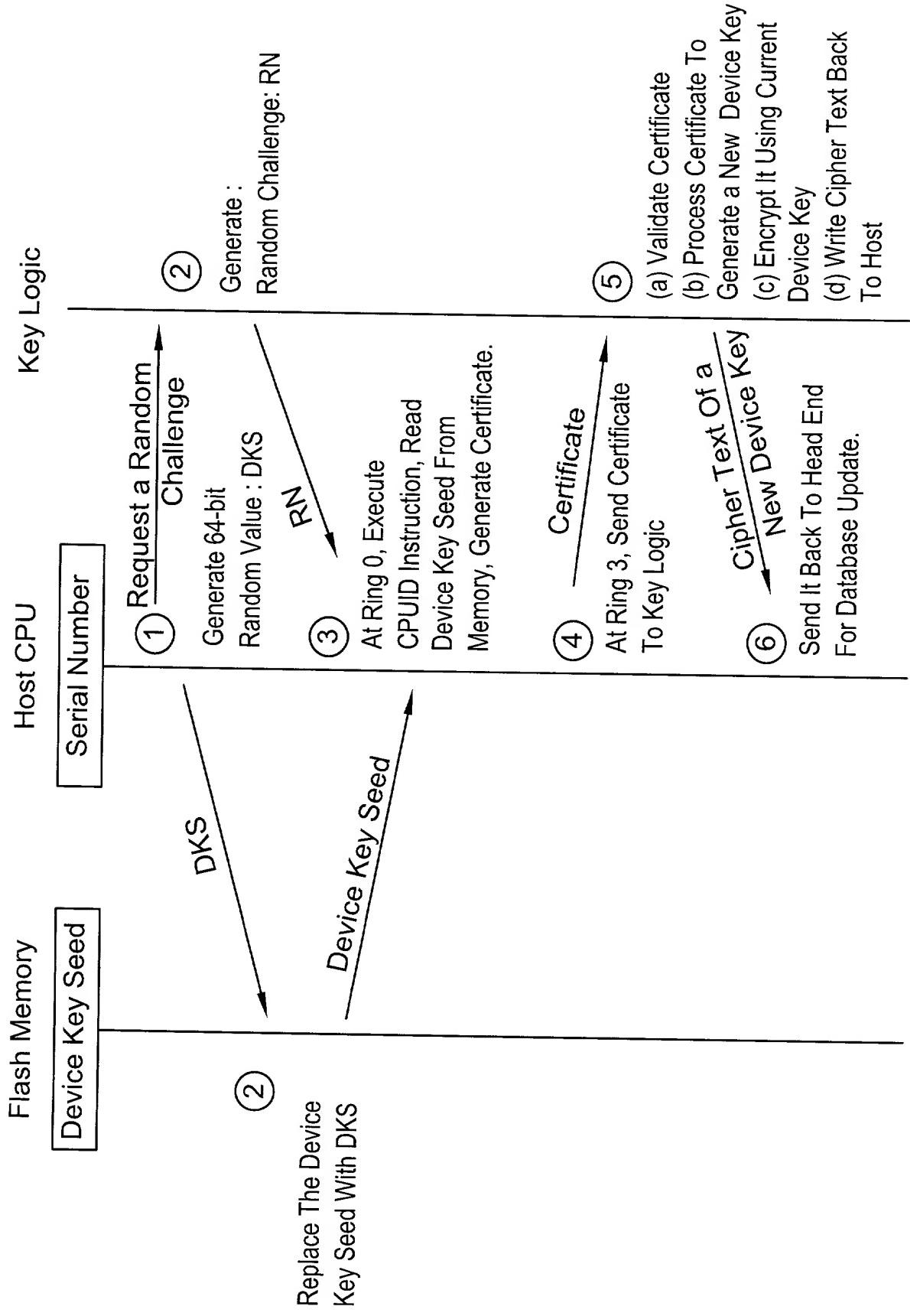


FIG. 2

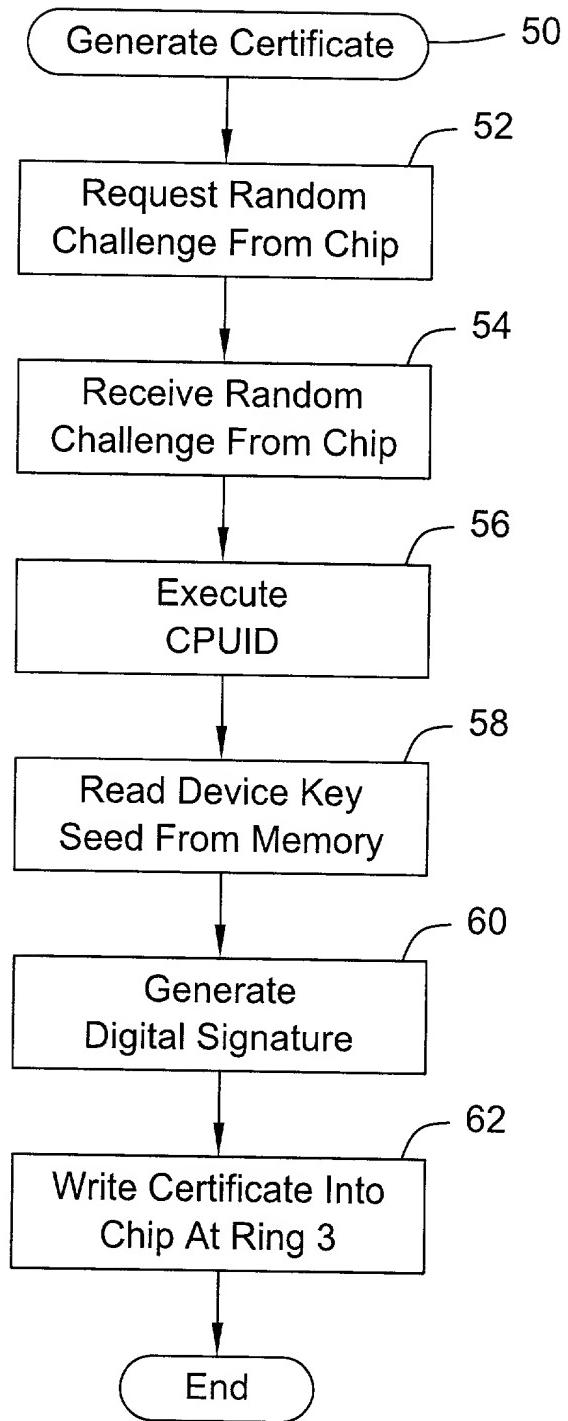


FIG. 3

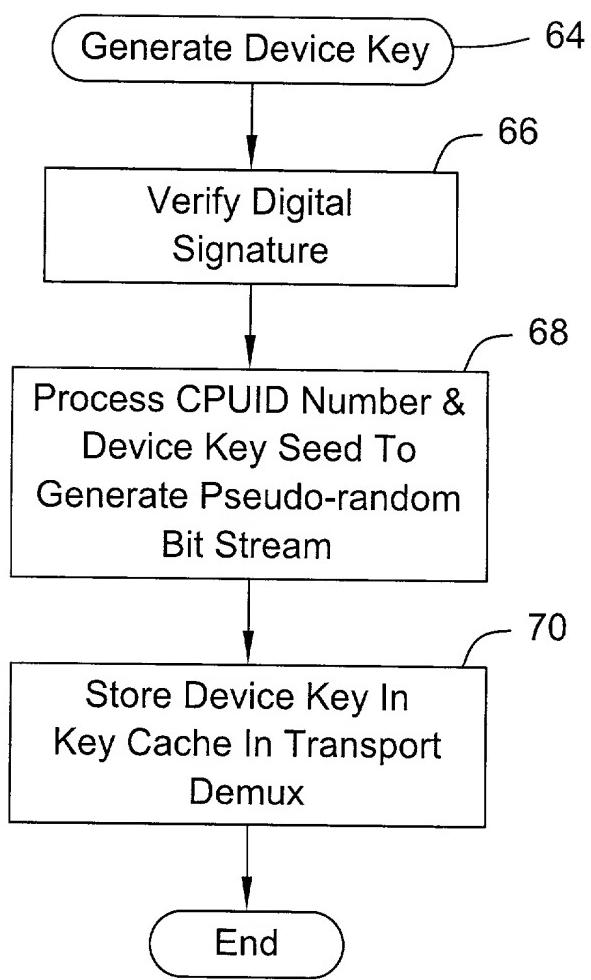


FIG. 4

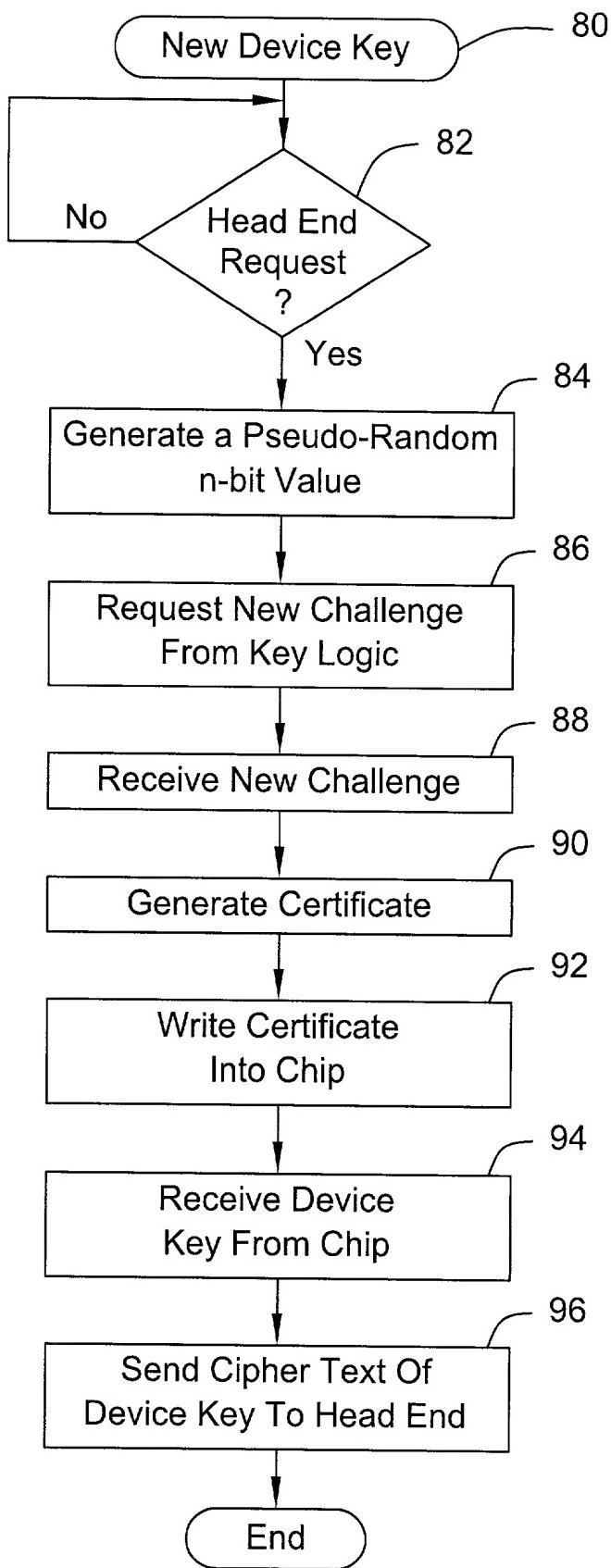


FIG. 5

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

ENABLING SECURE COMMUNICATIONS WITH A CLIENT

the specification of which

X	is attached hereto.
	was filed on _____ as
	United States Application Number _____
	or PCT International Application Number _____
	and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

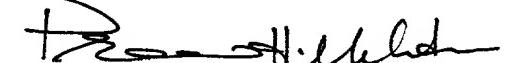
I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Number)	Filing Date	(Status-patented, pending, abandoned)
(Application Number)	Filing Date	(Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779 and Dan C. Hu, Reg. No. 40,025 my patent attorneys, of TROP, PRUNER & HU, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Mirho, Charles A.; Registration No. 41,199; Novakoski, Leo V.; Registration No. 37,198; Reynolds, Thomas C.; Registration No. 32,488; Seddon, Kenneth M.; Registration No. 43,105; Seeley, Mark; Registration No. 32,299; Skabrat, Steven P.; Registration No. 36,279; Skaist, Howard A.; Registration No. 36,008; Su, Gene I.; Registration No. 45,140; Wells, Calvin E.; Registration No. 43,256; Werner, Raymond J.; Registration No. 34,752; Winkle, Robert G.; Registration No. 37,474; and Young, Charles K.; Registration No. 39,435 my patent attorneys, of INTEL CORPORATION with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Timothy N. Trop, TROP, PRUNER & HU, P.C., 8554 Katy Freeway, Ste. 100, Houston, TX 77024 and direct telephone calls to Timothy N. Trop, (713) 468-8880.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor: MINDA ZHANG	
Inventor's Signature: 	Date: <i>July 25, 2000</i>
Residence: HUDSON, MASSACHUSETTS	Citizenship: P.R. CHINA
Post Office Address: 77 REED ROAD, HUDSON, MASSACHUSETTS 01749-2095	
Full Name of Second/Joint Inventor: PRANAV H. MEHTA	
Inventor's Signature: 	Date: <i>Sept 27, 2000</i>
Residence: CHANDLER, ARIZONA	Citizenship: INDIA
Post Office Address: 4183 W. BART DRIVE, CHANDLER, ARIZONA 85226	

INTL-0444 -US (P9444)